WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a copper interconnect line buried in an interlayer insulating film provided on a semiconductor substrate; and

a pad area connected to said copper interconnect line, wherein

said pad area comprises:

copper metal integrated with said copper interconnect line; and

aluminum alloy at least partially buried in said copper metal.

2. The semiconductor device according to claim 1, wherein

said aluminum alloy is entirely buried in said copper metal.

3. The semiconductor device according to claim 1, wherein

a bottom surface of said aluminum alloy buried in said copper metal reaches said interlayer insulating film.

4. The semiconductor device according to claim 1, wherein

said pad area comprises a titanium alloy layer provided at least on a surface of said aluminum alloy buried in said copper metal.

5. The semiconductor device according to claim 1, wherein

said pad area comprises a compound layer provided at least on a surface of said aluminum alloy buried in said copper metal, said compound layer including titanium alloy, copper and aluminum.

6. A semiconductor device, comprising:

a copper interconnect line buried in an interlayer insulating film provided on a semiconductor substrate; and

a pad area connected to said copper interconnect line, wherein

said pad area comprises:

copper metal integrated with said copper interconnect line; and

aluminum alloy contacting said copper metal, said aluminum alloy being at least partially buried in said interlayer insulating film.

7. The semiconductor device according to claim 6, wherein

said pad area comprises a titanium alloy layer provided at least on a surface of said aluminum alloy buried in said interlayer insulating film.

8. The semiconductor device according to claim 6, wherein

said pad area comprises a compound layer provided at least on a surface of said aluminum alloy buried in said interlayer insulating film, said compound layer including titanium alloy, copper and aluminum.

9. A method of manufacturing a semiconductor device, comprising the steps of:

(a) defining a trench in an interlayer insulating film to form an interconnect line and a pad area, said interlayer insulating film being provided on a semiconductor substrate;

(b) depositing copper over said semiconductor substrate to the extent that said trench to form said pad area is not totally filled;

(c) after said step (b), depositing aluminum alloy over said semiconductor substrate, to completely fill said trench to form said pad area; and

(d) removing said copper and said aluminum alloy while keeping said copper and said aluminum alloy in said trench to remain, to form said interconnect line and said pad area in said trench.

10. The method according to claim 9, further comprising the step of:

(e) between said steps (b) and (c), depositing titanium alloy over said semiconductor substrate to the extent that said trench to form said pad area is not totally filled, wherein

said step (d) further removes said titanium alloy while keeping said titanium alloy in said trench to remain.

11. The method according to claim 10, further comprising the step of:

(f) after said step (c), performing thermal processing to cause reaction between said titanium alloy, said copper and said aluminum alloy.

12. A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a copper interconnect line by a damascene process to be buried in an interlayer insulating film provided on a semiconductor substrate;

(b) defining an opening in said interlayer insulating film in such a manner that said opening is in contact with said buried interconnect line;

(c) depositing aluminum alloy to completely fill said opening; and

(d) removing said aluminum alloy while keeping said aluminum alloy at least in

said opening to remain, to form a pad area including said aluminum alloy.

13. The method according to claim 12, wherein

said buried interconnect line formed in said step (a) has an annular shape surrounding said opening defined in said step (b).

14. The method according to claim 12, further comprising the step of:

(e) between said steps (b) and (c), depositing titanium alloy over said semiconductor substrate to the extent that said opening is not completely filled, wherein

said step (d) further removes said titanium alloy while keeping said titanium alloy in said opening to remain.

15. The method according to claim 14, further comprising the step of:

(f) after said step (c), performing thermal processing to cause reaction between said titanium alloy, said copper and said aluminum alloy.